AMENDMENT TO CLAIMS

1-4. (Canceled)

5. (New) A semiconductor integrated circuit device comprising:

a silicon substrate;

a plurality of internal circuits each formed on an element region of the silicon substrate;

a first input/output (I/O) cell formed on an I/O cell region of the silicon substrate, the first I/O cell including a first I/O circuit, a first electrode portion horizontally spaced apart from the first I/O circuit with respect to the silicon substrate and a second electrode portion formed on the first I/O circuit, the first electrode portion and the second electrode portion electrically connected to each other and electrically connected to a first internal circuit of the plurality of internal circuits;

a second I/O cell formed on the I/O cell region of the silicon substrate, the second I/O cell including a second I/O circuit and a third electrode portion formed on the second I/O circuit, the third electrode portion electrically connected to a second internal circuit of the plurality of internal circuits; and

an interlayer insulating film formed on the plurality of internal circuits, the first I/O cell and the second I/O cell and exposing the first electrode portion as a probing pad, the second electrode portion as a first terminal pad and the third electrode portion as a second terminal pad.

6. (New) The semiconductor integrated circuit device according to claim 5, wherein an area of each of the first terminal pad and the second terminal pad is smaller than that of the probing pad.

7. (New) The semiconductor integrated circuit device according to claim 5, wherein the first internal circuit is a DRAM including a fuse element electrically connected to the probing pad.

8. (New) The semiconductor integrated circuit device according to claim 5, further comprising:

an insulating protective film formed on a surface of the interlayer insulating film, the insulating protective film covering the probing pad from above with respect to the silicon substrate and exposing the first terminal pad and the second terminal pad;

a rearrangement wiring formed on a surface of the insulating protective film and electrically connected to either the first terminal pad or the second terminal pad; and

a solder bump formed on the rearrangement wiring.

9. (New) The semiconductor integrated circuit device according to claim 8, further comprising a barrier metal layer formed between the solder bump and a surface of the rearrangement wiring.

10. (New) The semiconductor integrated circuit device according to claim 5, further comprising a plurality of I/O cells each formed on the I/O cell region of the silicon substrate and placed along one side of the silicon substrate, and

wherein each of the plurality of I/O cells is the second I/O cell.

11. (New) A manufacturing method of a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising:

a silicon substrate;

a plurality of internal circuits each formed on an element region of the silicon substrate;

a first input/output (I/O) cell formed on an I/O cell region of the silicon substrate, the first I/O cell including a first I/O circuit, a first electrode portion horizontally spaced apart from the first I/O circuit with respect to the silicon substrate and a second electrode portion formed on the first I/O circuit, the first electrode portion and the second electrode portion electrically connected to each other and electrically connected to a fuse element included in a DRAM of the plurality of internal circuits;

a second I/O cell formed on the I/O cell region of the silicon substrate, the second I/O cell including a second I/O circuit and a third electrode portion formed on the second I/O circuit, the third electrode portion electrically connected to a second internal circuit of the plurality of internal circuits; and

an interlayer insulating film formed on the plurality of internal circuits, the first I/O cell and the second I/O cell and exposing the first electrode portion as a probing pad, the second electrode portion as a first terminal pad and the third electrode portion as a second terminal pad,

the manufacturing method comprising the steps of:

cutting the fuse element via the probing pad when the DRAM characteristic is problematic;

forming an insulating protective film on a surface of the interlayer insulating film so that the insulating protective film covers the probing pad from above with respect to the silicon substrate and exposes the first terminal pad and the second terminal pad;

forming a rearrangement wiring on a surface of the insulating protective film so that the rearrangement wiring electrically connects to either the first terminal pad or the second terminal pad; and

forming a solder bump on the rearrangement wiring.

12. (New) The manufacturing method according to claim 11, further comprising the step of forming a barrier metal layer between the solder bump and a surface of the rearrangement wiring.